Abstract

"Channel Decoder for a Digital Broadcast Receiver"

A channel decoder for a digital broadcast receiver according to the present invention enables the use of the packet synchronization status available within such a channel decoder, i. e. within the synchronization byte detector (1) included therein, for other than synchronization purposes. Generally, the present invention discloses the use of the packet synchronization status, namely a lock detected output signal supplied by the synchronization byte detector (1) to assign the amount of processing power within the channel decoder and/or the whole digital broadcast receiver. In particular the disabling/ enabling of the error correction (3) and/or all processing stages following within the channel decoder and/or the whole receiver, the switching of the loop bandwidth of the clock and carrier recovery loop (2) and/or the switching of the clock/carrier phase detectors (2) to implementations that work only in locked mode, but in this case better than the robust implementations used for acquisition is disclosed as well as the supply of the lock detected output signal.

(Fig. 1)